

Design of 4:16 decoder using reversible logic gates

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ABSTRACT

Reversible logic has received great importance in the recent years because of its feature of reduction in power dissipation. It finds application in low power digital designs, quantum computing, nanotechnology, DNA computing etc. Large number of researches are currently ongoing on sequential and combinational circuits using reversible logic. Decoders are one of the most important circuits used in combinational logic. Different approaches have been proposed for their design. In this article, we have proposed a novel design of 4:16.

Keywords: Reversible logic, decoder, quantum cost

I. INTRODUCTION

Landauer [1] showed that the heat generated during computation is not due to the processing of bits, but due to the loss of information. Wiping of each bit of information causes $kT \ln 2$ amount of heat dissipation where k is Boltzmann constant = 1.3805×10^{-23} J/K and T is the temperature in absolute scale. While this heat may be negligible for a single wipe of information, in this modern VLSI design, where many chips are arranged in small region and millions of instructions are processed per second, the information loss and consequently the heat generation is formidable.

Bennet [2] later showed that this heat dissipation can be avoided by using reversible computation. This proof by Bennett has led to an extensive research on reversible logic. Most prominent applications of reversible logic are seen in quantum computation, low Power CMOS Design, nanotechnology and DNA computing.

Quantum networks are composed of quantum logic gates each gate performing an elementary unitary operation on one, two or more than two state quantum systems called qubits. Each qubit represent an elementary unit of information corresponding to the classical bit values 0 and 1. Any unitary operation is reversible and hence quantum arithmetic must be built from reversible logic components [3].

Quantum cost, delay number of constant inputs and garbage outputs are the most important cost metrics of reversible computing. Garbage outputs are the outputs which are present only to maintain reversibility and do not perform any useful operations. Number of gates is not a good measure of cost, since more than one gate can be taken together to form a new gate, thus reducing the gate count.

Quantum gates involve many qubits are extremely difficult to build. Hence quantum cost is an important metric to build quantum gates. Quantum cost is the number of elementary quantum gates required to build the gate. 1×1 reversible gates viz. NOT gate have quantum cost 0 while 2×2 gates viz. Controller-C, Controlled-V, Controlled- V^+ , CNOT gate etc. have quantum cost 1 [4].

Design of Combinational sequential circuits have been ongoing for some time. Various proposals are given for the design of adders, subtractors [5], multiplexers [6], decoders etc. Recently a new reversible SG gate [7] has been proposed. Though the provided design is of 4 qubit gate, the encoding logic enables the gate to be extended to n qubits gate for any $n > 4$ and the authors have shown this gate to be universal.

In this paper, we have proposed a novel design of 4:16 whose quantum cost is less than the previous design

II. BASIC REVERSIBLE GATES

Reversible gates are $n \times n$ logic gates where the input vectors $I = (i_1, i_2, \dots, i_n)$ are mapped to the output vectors $O = (o_1, o_2, \dots, o_n)$. The mapping is bijective, i.e., every input is mapped to an output and every output has a unique input mapped to it. Thus the outputs of reversible gates are permutations of the inputs. Fan-outs are not allowed in reversible circuit since they violate one-to-one mapping. Some basic reversible gates are introduced in this section.

A. NOT Gate

The Simplest reversible gate is NOT gate. It is a 1×1 gate with quantum cost 0. NOT gate simply flips the input as shown in Fig.1.

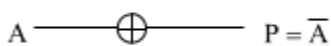


Fig. 1. NOT gate

B. Controlled-V and Controlled-V† Gate

Controlled-V and Controlled-V† gates are 2*2 reversible gates with quantum cost 1. In Controlled-V gate, if the control signal A = 0, then the second input B passes unchanged. However, if A = 1, then the unitary operation $\frac{i+1}{2} \begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}$ is applied to the input B. Controlled-V† gate is simple the conjugate transpose of Controlled-V gate.

Controlled-V and Controlled-V† have the following properties

$$\begin{aligned} V \times V &= \text{NOT} \\ V \times V^\dagger &= V^\dagger \times V = I \\ V^\dagger \times V^\dagger &= \text{NOT} \end{aligned}$$

Hence controlled-V is also called square root of NOT gate. Quantum implementation of V and V† are shown in Fig. 2

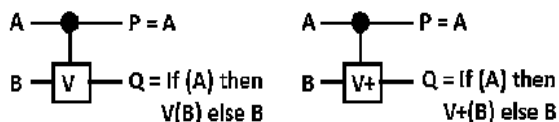


Fig. 2. Quantum Implementation of Controlled-V and Controlled-V† Gate

C. Feynman Gate

Fig. 3 shows the block diagram and the quantum implementation of Feynman Gate [8], also called Controlled-Not (CNOT) gate. It is a 2*2 gate and its quantum cost is 1. The inputs are A and B and the outputs P = A and Q = A ⊕ B.

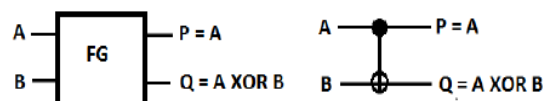


Fig. 3. Block diagram and Quantum representation of Feynman gate

D. Peres gate

Fig. 4 shows the block diagram and quantum realization of Peres Gate [9]. It is a 3*3 gate with inputs A, B and C and the outputs P = A, Q = A ⊕ B and R = AB ⊕ C. Its quantum cost is 4 since four 2*2 gates are required for its realization.

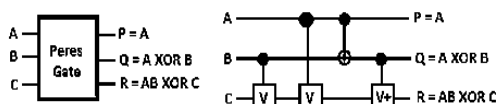


Fig. 4. Block diagram and quantum representation of Peres gate.

E. TR gate

Fig. 5 shows the block diagram and quantum realization of TR Gate[10]. It is a 3*3

gate with inputs A, B and C and outputs P = A, Q = A ⊕ B and R = AB' ⊕ C. Its quantum cost is 4 since four 2*2 gates are required for its realization.

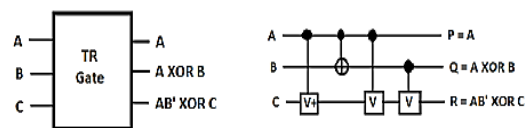


Fig. 5 Block diagram and quantum implementation of TR gate.

F. Fredkin Gate

Fig. 6 shows the block diagram and quantum realization of Fredkin Gate [11]. It is a 3*3 gate with inputs A, B and C and outputs P = A, Q = AB + A'C and R = A'B + AC. Its quantum cost is 5 since five 2*2 gates are required for its realization.

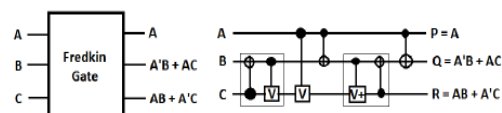
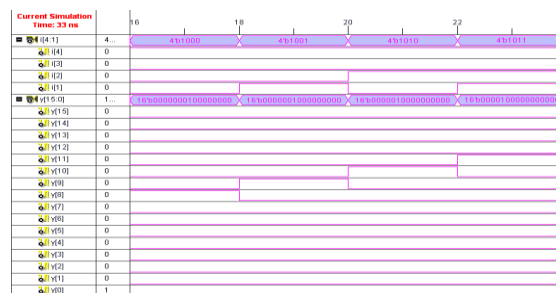
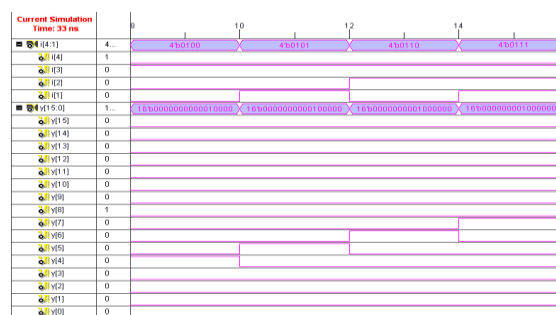
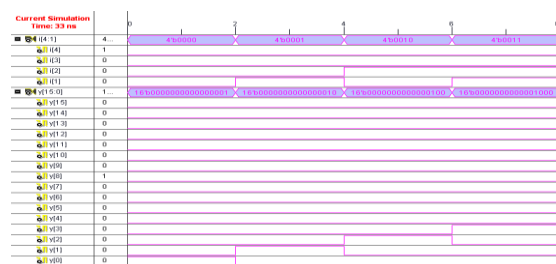
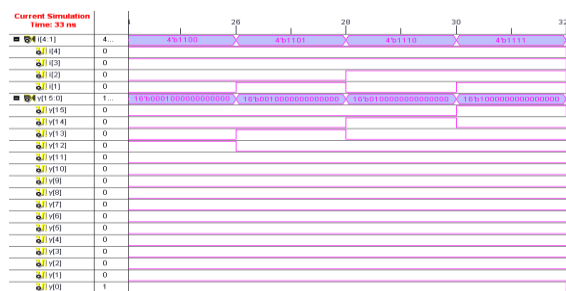


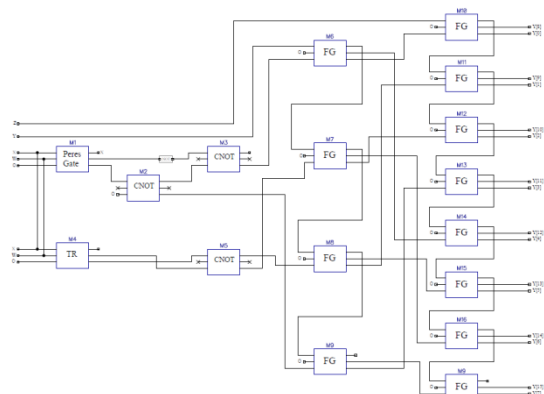
Fig. 6. Block diagram and quantum implementation of Fredkin Gate.

III. SIMULATION RESULTS.





IV. SCHEMATIC



W, X, Y, Z Are the inputs

V. CONCLUSION

In this article, we have proposed a novel design of 4:16. We have shown that the quantum cost of a $n : 2n$ decoder will be less by 4 if we use our proposed 4:16 decoder block.

The increase in the number of Fredkin gates is exponentially higher for increase in a single input. Though for n inputs, the number of outputs is 2 number of outputs, the increase in gates is linear. However, by using any other gates like Toffoli, Peres or TR gate, the number of gates will be twice as high and hence the quantum cost will be nearly twice. The number of garbage outputs also increases in the same manner since each Fredkin gate has one garbage output for this architecture.

The generalised design cannot be optimised any further by using the basic gates like Peres, TR or Toffli. However, further research interest may be to propose new gates that can be used to replace Fredkin gates in higher dimensional decoders, resulting in decrease of quantum cost.

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